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DATA SHEET

BF998WR
N-channel dual-gate MOS-FET

Product specification
Supersedes data of 1995 Apr 25
File under Discrete Semiconductors, SC07

1997 Sep 05

Philips
Semiconductors

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N-channel dual-gate MOS-FET BF998WR

FEATURES

- High forward transfer admittance
- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz.

APPLICATIONS

- VHF and UHF applications with 12 V supply voltage, such as television tuners and professional communications equipment.

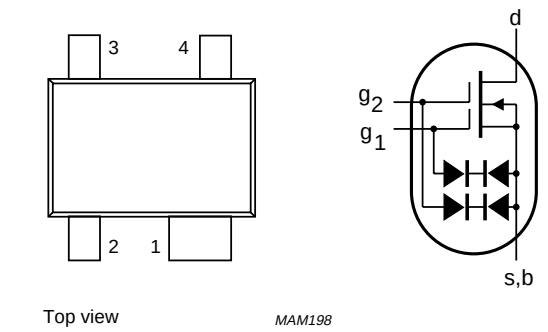
DESCRIPTION

Depletion type field-effect transistor in a plastic microminiature SOT343R package with source and substrate interconnected. The transistor is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source
2	d	drain
3	g_2	gate 2
4	g_1	gate 1



Marking code: MB.

Fig.1 Simplified outline (SOT343R) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	12	V
I_D	drain current		–	–	30	mA
P_{tot}	total power dissipation		–	–	300	mW
T_j	operating junction temperature		–	–	150	°C
$\lvert y_{fs} \rvert$	forward transfer admittance		–	24	–	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1		–	2.1	–	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	–	25	–	fF
F	noise figure	f = 800 MHz	–	1	–	dB

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	12	V
I_D	drain current		–	30	mA
I_{G1}	gate 1 current		–	±10	mA
I_{G2}	gate 2 current		–	±10	mA
P_{tot}	total power dissipation	up to T_{amb} = 45 °C; see Fig.2; note 1	–	300	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	+150	°C

Note

1. Device mounted on a printed-circuit board.

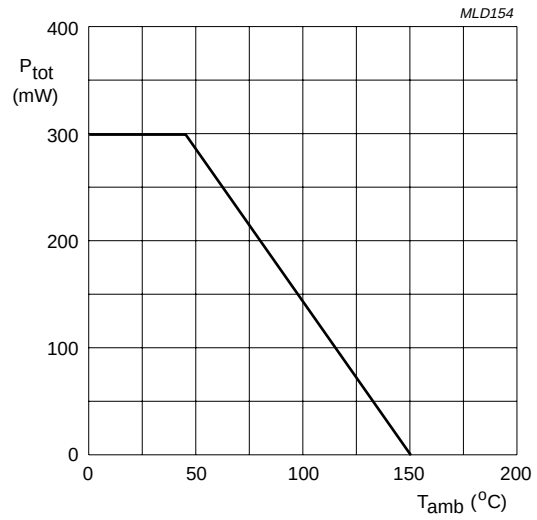


Fig.2 Power derating curve.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	350	K/W
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	note 2; T_s = 90 °C	200	K/W

Notes

1. Device mounted on a printed-circuit board.
2. T_s is the temperature at the soldering point of the source lead.

STATIC CHARACTERISTICS

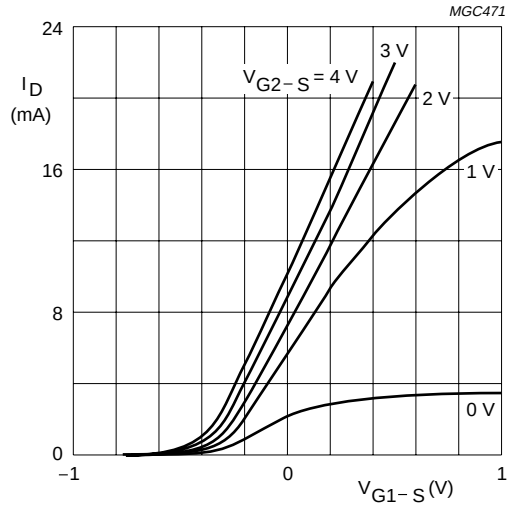
T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)G1\text{-}SS}$	gate 1-source breakdown voltage	$V_{G2\text{-}S}$ = V_{DS} = 0; $I_{G1\text{-}S}$ = 10 mA	6	20	V
$V_{(BR)G2\text{-}SS}$	gate 2-source breakdown voltage	$V_{G1\text{-}S}$ = V_{DS} = 0; $I_{G2\text{-}S}$ = 10 mA	6	20	V
$V_{(P)G1\text{-}S}$	gate 1-source cut-off voltage	$V_{G2\text{-}S}$ = 4 V; V_{DS} = 8 V; I_D = 20 μA	–	–2.5	V
$V_{(P)G2\text{-}S}$	gate 2-source cut-off voltage	$V_{G1\text{-}S}$ = 0; V_{DS} = 8 V; I_D = 20 μA	–	–2	V
I_{DSS}	drain-source current	$V_{G2\text{-}S}$ = 4 V; V_{DS} = 8 V; $V_{G1\text{-}S}$ = 0	2	18	mA
$I_{G1\text{-}SS}$	gate 1 cut-off current	$V_{G2\text{-}S}$ = V_{DS} = 0; $V_{G1\text{-}S}$ = 5 V	–	50	nA
$I_{G2\text{-}SS}$	gate 2 cut-off current	$V_{G1\text{-}S}$ = V_{DS} = 0; $V_{G2\text{-}S}$ = 5 V	–	50	nA

DYNAMIC CHARACTERISTICS

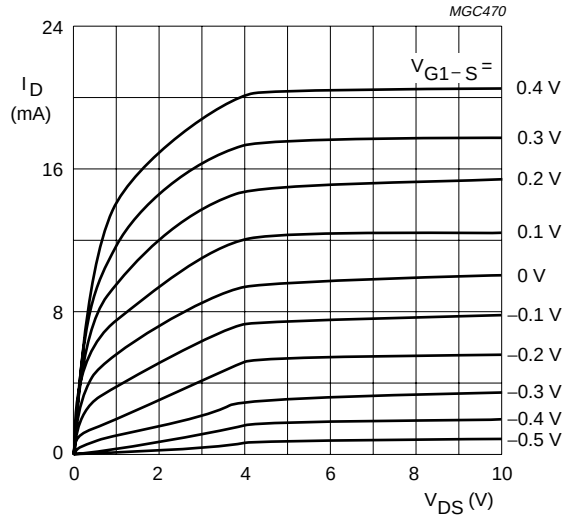
Common source; T_{amb} = 25 °C; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA; V_{DS} = 8 V; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert y_{fs}\rvert$	forward transfer admittance	pulsed; T_j = 25 °C	22	25	–	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	f = 1 MHz	–	2.1	2.5	pF
$C_{ig2\text{-}s}$	input capacitance at gate 2	f = 1 MHz	–	1.2	–	pF
C_{os}	drain-source capacitance	f = 1 MHz	–	1.05	–	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	–	25	–	fF
F	noise figure	f = 200 MHz; G_S = 2 mS; B_S = B_{Sopt}	–	0.6	–	dB
		f = 800 MHz; G_S = 3.3 mS; B_S = B_{Sopt}	–	1	–	dB



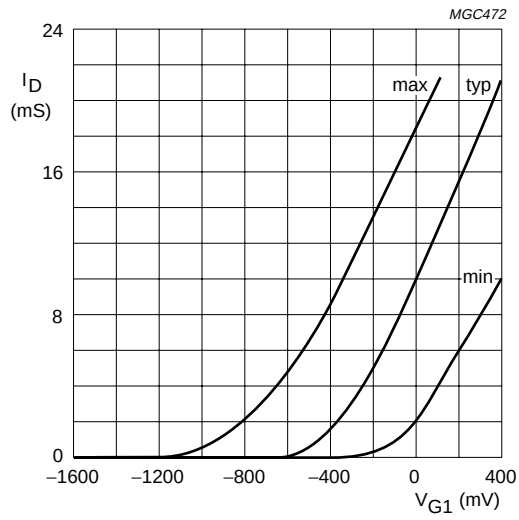
V_{DS} = 8 V.
T_{amb} = 25 °C.

Fig.3 Transfer characteristics; typical values.



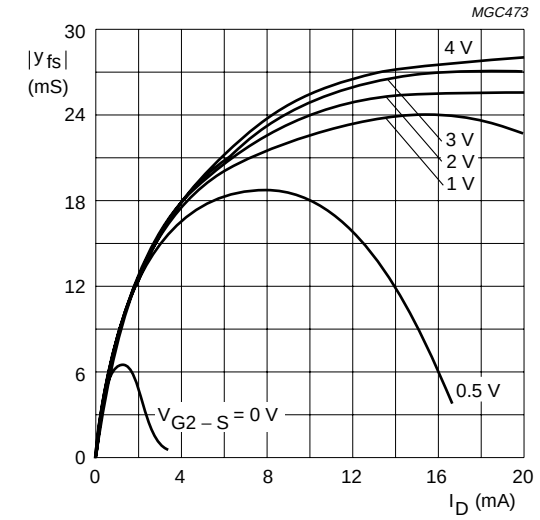
$V_{G2\text{-}S}$ = 4 V.
T_{amb} = 25 °C.

Fig.4 Output characteristics; typical values.



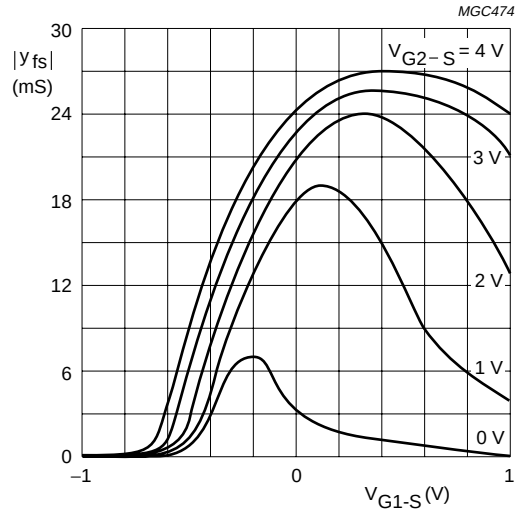
V_{DS} = 8 V; V_{G2} = 4 V; T_{amb} = 25 °C.

Fig.5 Drain current as a function of gate 1 voltage; typical values.



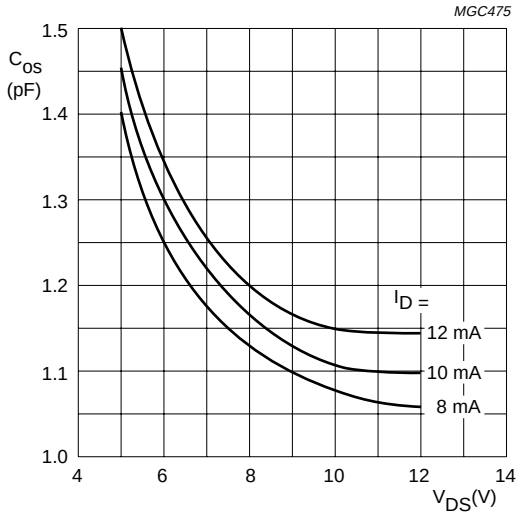
V_{DS} = 8 V; T_{amb} = 25 °C.

Fig.6 Forward transfer admittance as a function of drain current; typical values.



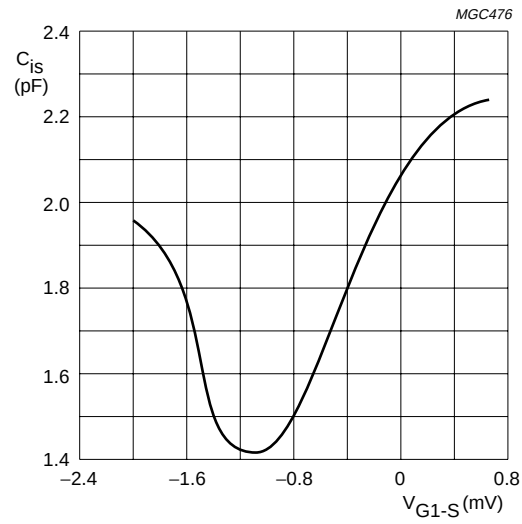
V_{DS} = 8 V; T_{amb} = 25 °C.

Fig.7 Forward transfer admittance as a function of gate 1 voltage; typical values.



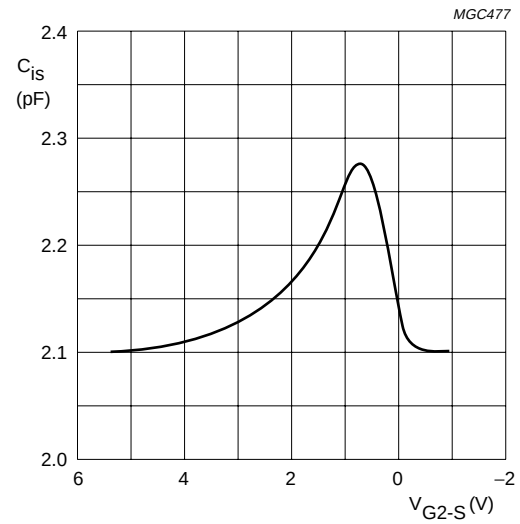
V_{G2-S} = 4 V; f = 1 MHz; T_{amb} = 25 °C.

Fig.8 Output capacitance as a function of drain-source voltage; typical values.



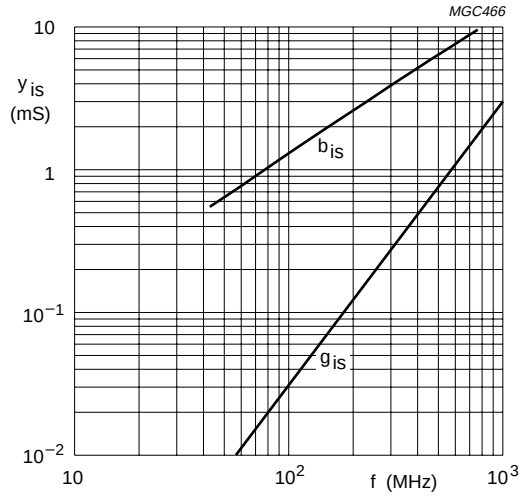
V_{DS} = 8 V; V_{G2-S} = 4 V; f = 1 MHz; T_{amb} = 25 °C.

Fig.9 Gate 1 input capacitance as a function of gate 1-source voltage; typical values.



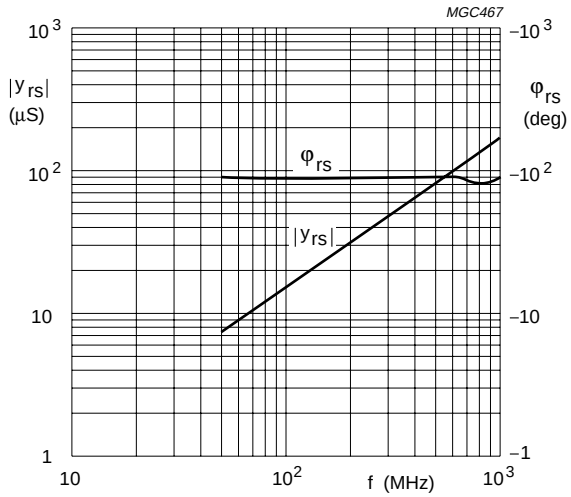
V_{DS} = 8 V; V_{G1-S} = 0 V; f = 1 MHz; T_{amb} = 25 °C.

Fig.10 Gate 1 input capacitance as a function of gate 2-source voltage; typical values.



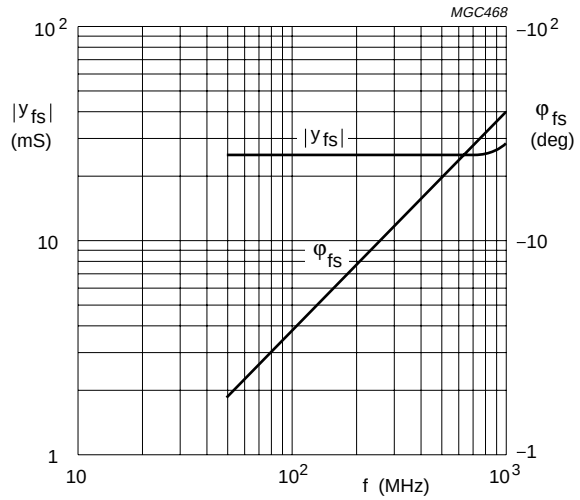
V_{DS} = 8 V; V_{G2-S} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.11 Input admittance as a function of the frequency; typical values.



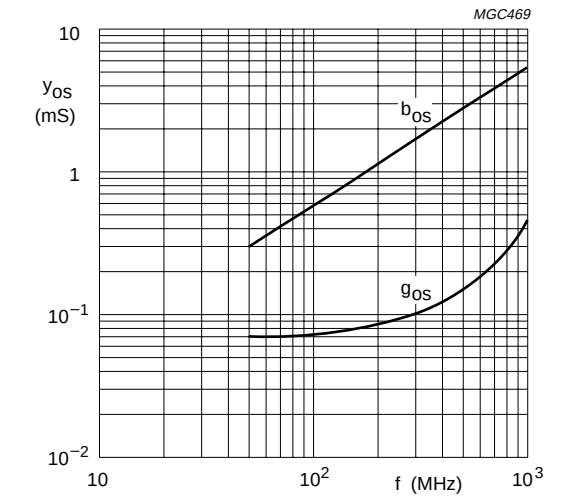
V_{DS} = 8 V; V_{G2-S} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.12 Reverse transfer admittance and phase as a function of frequency; typical values.



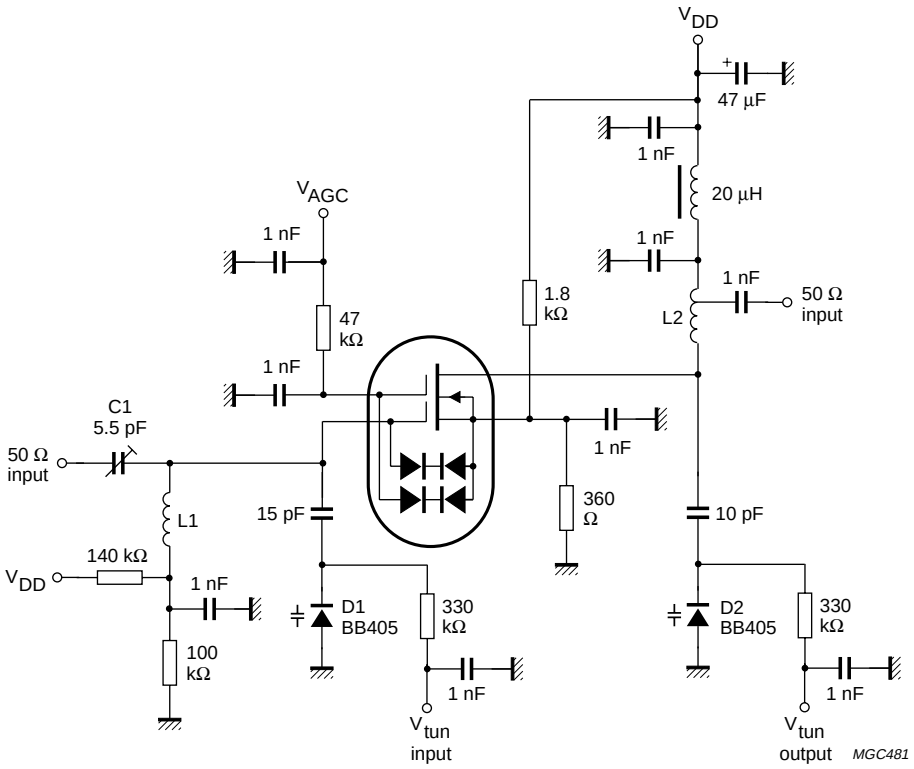
V_{DS} = 8 V; V_{G2-S} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.13 Forward transfer admittance and phase as a function of frequency; typical values.



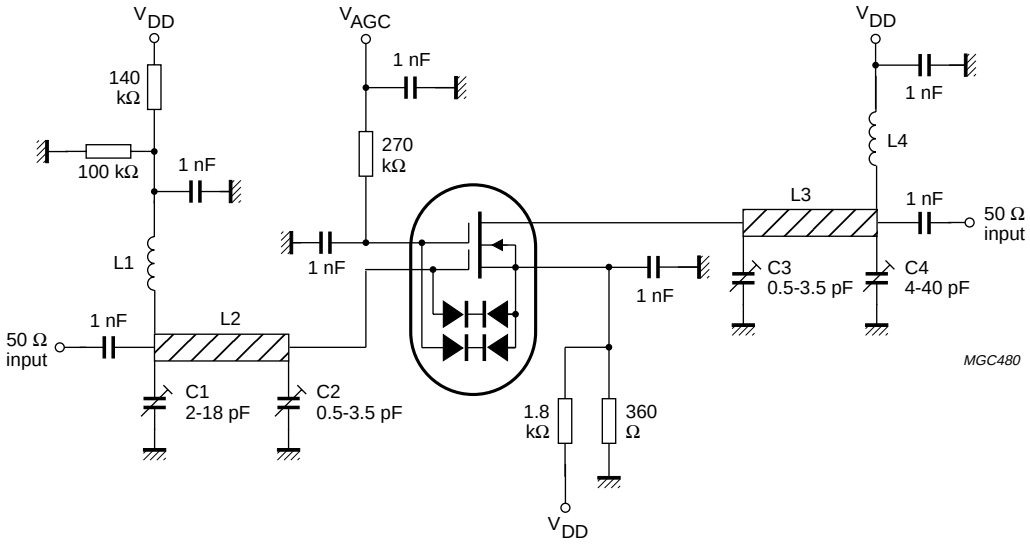
V_{DS} = 8 V; V_{G2-S} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.14 Output admittance as a function of the frequency; typical values.



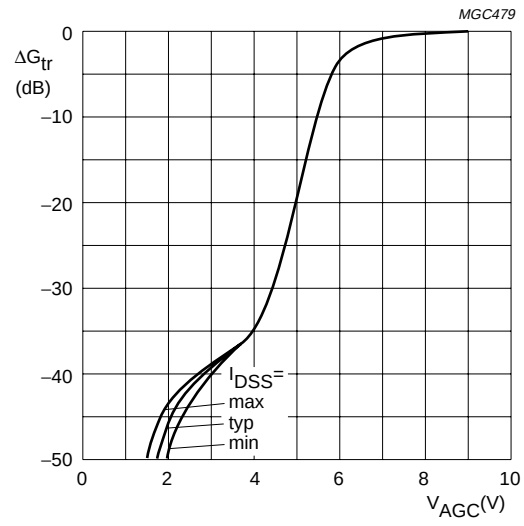
V_{DD} = 12 V; G_S = 2 mS; G_L = 0.5 mS.
L1 = 45 nH; 4 turns 0.8 mm copper wire, internal diameter 4 mm.
L2 = 160 nH; 3 turns 0.8 mm copper wire, internal diameter 8 mm.
Tapped at approximately half a turn from the cold side, to adjust G_L = 0.5 mS. C1 adjusted for G_S = 2 mS.

Fig.15 Gain control testcircuit at f = 200 MHz.



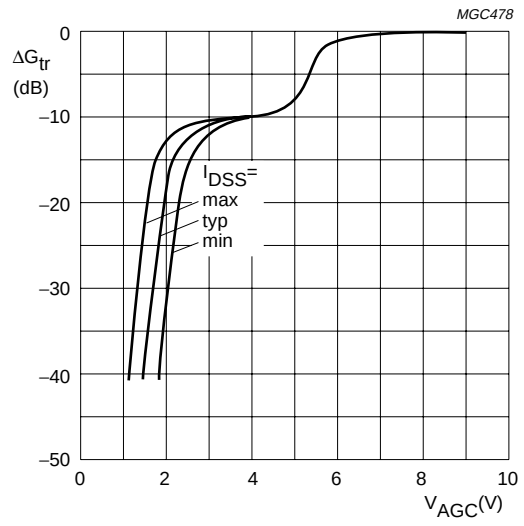
V_{DD} = 12 V; G_S = 3.3 mS; G_L = 1 mS.
L1 = L4 = 200 nH; 11 turns 0.5 mm copper wire, without spacing, internal diameter 3 mm.
L2 = 2 cm, silvered 0.8 mm copper wire, 4 mm above ground plane.
L3 = 2 cm, silvered 0.5 mm copper wire, 4 mm above ground plane.

Fig.16 Gain control test circuit at f = 800 MHz.



V_{DD} = 12 V; f = 200 MHz; T_{amb} = 25 °C.

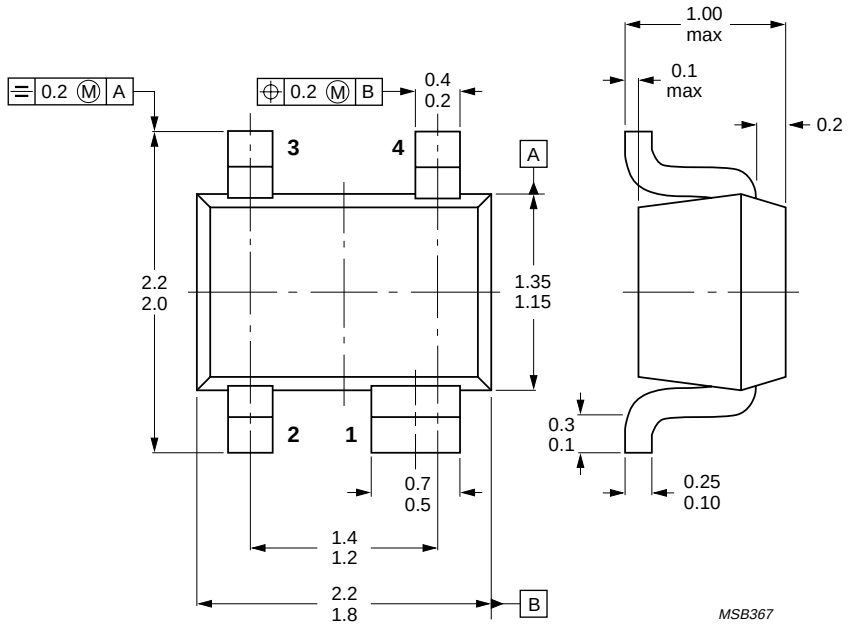
Fig.17 Automatic gain control characteristics measured in circuit of Fig.15.



V_{DD} = 12 V; f = 800 MHz; T_{amb} = 25 °C.

Fig.18 Automatic gain control characteristics measured in circuit of Fig.16.

PACKAGE OUTLINE



Dimensions in mm.

Fig.19 SOT343R.

DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 160 1010,
Fax. +43 160 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 0044

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615800, Fax. +358 9 61580920

France: 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: see Singapore

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Rua do Rocio 220, 5th floor, Suite 51,
04552-903 São Paulo, SÃO PAULO - SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 829 1849

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 3 301 6312, Fax. +34 3 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 632 2000, Fax. +46 8 632 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2686, Fax. +41 1 481 7730

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381

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